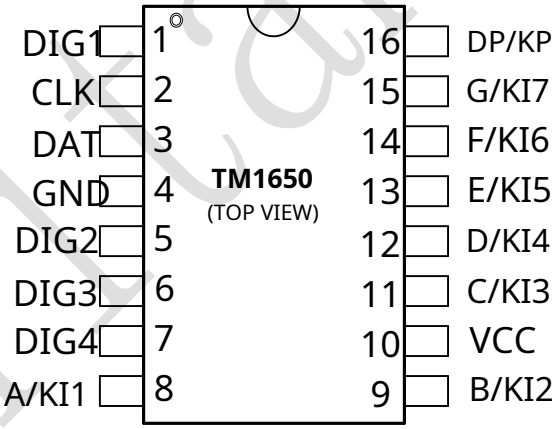
1. Overview

TM1650 is a LED (light-emitting diode display) drive control IC with keyboard scan interface, which integrates MCU digital interface, data latch, LED drive, keyboard scan and other circuits. This product has reliable quality, good stability and strong anti-interference ability. It is mainly suitable for digital tubes such as set-top boxes, household appliances (smart water heaters, microwave ovens, washing machines, air conditioners, induction cookers), electronic scales, smart meters, etc., and can be used in applications where 24 hours of long-term continuous work is required.

2. Features

- **Two display modes (8 segments x 4 digits and 7 segments x 4 digits)**
- **Support single key 7x4bit (28 keys) and combination keys (4 keys)**
- **8 levels of brightness adjustable**
- **Segment drive current greater than 25mA, bit drive current greater than 150mA**
- **High-speed 2-wire serial interface (CLK, DAT)**
- **Oscillation mode: built-in RC oscillation**
- **Built-in power-on reset circuit**
- **Built-in data latch circuit**
- **Support 3-5.5V power supply voltage**
- **Strong anti-interference ability**
- **Package type: SOP16, DIP16**

3. Pin Definition:

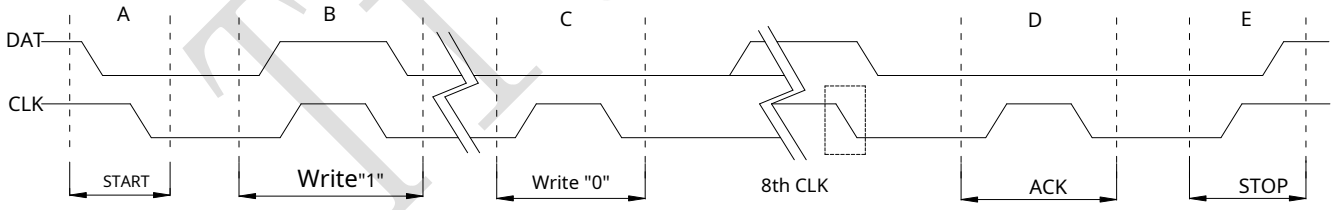


4. PinsFunction definition:

symbol	Pin Name	Pin Number	illustrate
CLK	Clock Input	2	2-wire serial interface data clock input, built-in Pull resistor
DAT	Data Input/Output	3	2-wire serial interface data input and output, built-in Pull-up open-drain mode
A/KI1-G/KI7	Segment output/key scan input	8-15	LED segment drive output, high level is effective; keyboard scan Scan input, high level valid, built-in pull-down.
DIG1-DIG4	Bit/key scan output	1, 5 6, 7	LED driver output, low level is effective; keyboard scan Scan output, high level valid
DP/KP	Segment output/key scan flag Output	16	LED segment drive output, high level is effective; keyboard scan Scanning mark output: When the 7-segment screen is on, if it is detected A valid key will output a low level of the flag
VCC	Logic Power Supply	10	Connect to positive power supply (3-5.5V)
GND	Logically	4	Connect to system ground

5. Communication timing format:

TM1650 uses the 2-wire serial transmission protocol communication shown in Figure 1:



picture1

1. Start signal (START)/end signal (STOP)

Start signal: Keep CLK at "1" level, DAT jumps from "1" to "0", which is considered as the start signal, such as (Figure 1) segment A; End signal: Keep CLK at "1" level, DAT jumps from "0" to "1", which is considered as the end signal, such as (Figure 1) segment E; **2. ACK signal**

If the communication is normal, after the 8th clock falling edge of the serial communication, TM1650 will actively pull DAT down until the rising edge of CLK is detected, and DAT will be released to the input state (for the chip), as shown in segment D of (Figure 1).

3. Write "1" and write "0"

Write "1": Keep DAT at "1" level, CLK jumps from "0" to "1", and then from "1" to "0", it is considered to be written "1" as shown in (Figure 1) Section B.

Write "0": Keep DAT at "0" level, CLK jumps from "0" to "1", and then from "1" to "0", it is considered to be written "0" as shown in (Figure

1) Segment C.

4. One byte (8 bits) data transmission format

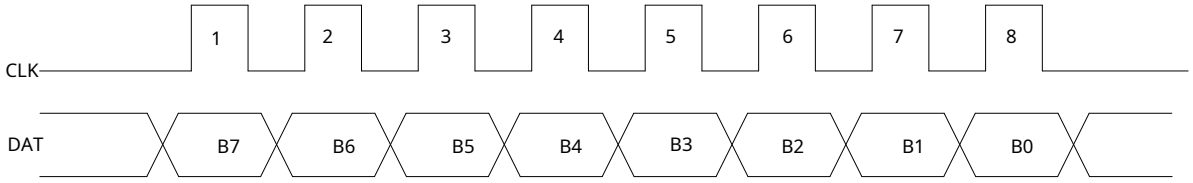
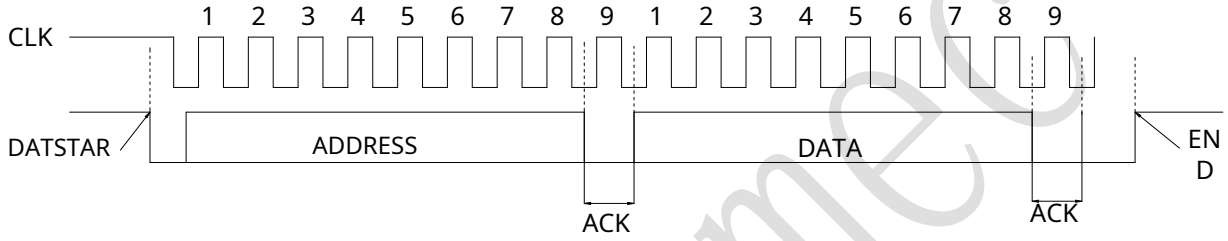


Figure 2

The transmission format of a byte of data is shown in Figure 2. When data is sent, the MSB is in front and the LSB is in the back, that is, the high bit is first. The data of the microprocessor communicates with TM1650 through a 2-wire serial interface. When CLK is high, the signal on DAT must remain unchanged; only when the clock signal on CLK is low, the signal on DAT can change. The start condition of data input is when CLK is high, DAT changes from high to low; the end condition is when CLK is high, DAT changes from low to high.

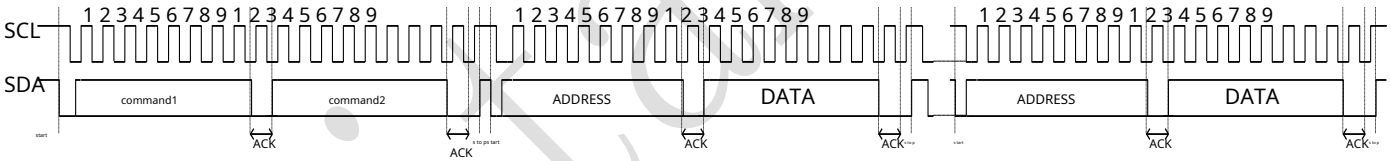
5. Write display operation



picture3Write Display Timing

ADDRESS: Display address (68H,6AH,6CH,6E);
DATA: Display data.

6. Complete operation sequence



picture4Complete timing

command1: System Commands48H;

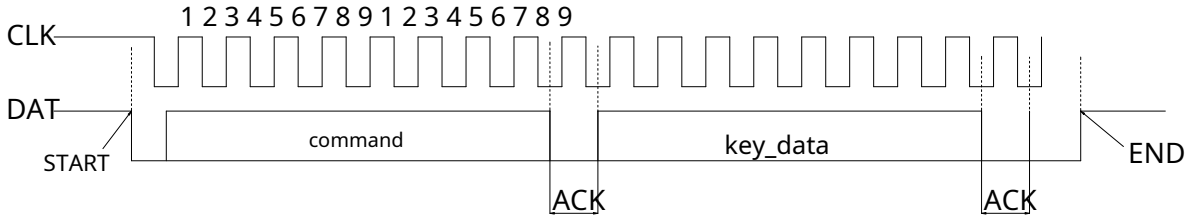
command2: System parameter settings;

ADDRESS: Display address (68H,6AH,6CH,6E);

DATA: Display data.

Note: 1. Setting system parameters and writing video memory data are two independent processes, and their order does not affect the actual application;

2. Each time you input a system command (48H) and a system parameter setting command, the system parameters will be changed. Please pay special attention to the standby command operation. **7. Read key sequence**



picture5Read button timing

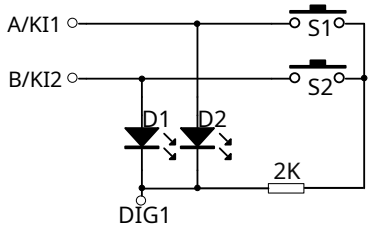
command: Read key commands4F;

key_data: Read key data (one byte).

Note: When reading a key, the data is fromTM1650Output toMCU, at this time withTM1650ofDATConnectedIOThe port must be set to input mode and released.

Release the bus; the key code is output from the high position first P7P6P5P4_P3P2P1P (0 The underscore makes it easier to distinguish between binary (B) and hexadecimal (H). The initial state is 0010_1110B (2E).TM1650Supports single and combined keystrokes.

Key drive circuit:DIGandKIThe feet should be connected in series2KΩResistance, must be ensured before reading the buttonTM1650The chip is in the scanning state, that is, it is in the display state.



picture6Key drive circuit

Output value when the button is pressed:**(P6=1 when the button is pressed)**

KI	DIG4	DIG3	DIG2	DIG1
A/KI1	47H	46H	45H	44H
B/KI2	4F	4EH	4DH	4CH
C/KI3	57H	56H	55H	54H
D/KI4	5F	5E	5DH	5CH
E/KI5	67H	66H	65H	64H
F/KI6	6FH	6E	6DH	6CH
G/KI7	77H	76H	75H	74H
KI1+KI2	7F	7E	7D	7CH

In the same DIG, the KI1+KI2 combination takes priority; in addition, if multiple keys are pressed at the same time, the key with the smallest code takes priority. If they are not pressed at the same time, the key pressed first takes priority.

Keyboard Scanning:

1 Supports keyboard scanning of up to 28 keys in a 4*7 matrix. During keyboard scanning, DIG is used for column scan output and KI is used for row scan input. 2 Insert keyboard scanning periodically in the display driver scanning process. During keyboard scanning, DIG1~DIG4 will output high level in turn, and the remaining pins will output low level. At this time, KI1~KI7 outputs are disabled. When no key is pressed, they are all pulled down to low level; when a key is pressed, for example, the key connecting DIG2 and KI2 is pressed, KI2 inputs high level when DIG2 outputs high level. In order to avoid bit errors caused by key jitter and external interference, the chip performs two keyboard scans inside. Only when the results of the two scans are the same, the key will be confirmed to be valid. Therefore, the key pressing time is greater than 2 key scan cycles.

3 The key code is 8 bits, bit 7 (P7) is always 0, bit 2 (P2) is always 1, bits 1 and 0 are column scan codes, bits 5 to 3 (P5P4P3) are row scan codes, and bit 6 (P6) is the status code (key pressed is 1, key released is 0).

For example, when the key connecting DIG2 and KI5 is pressed, the key code is 65H or 01101001B; when the key is released, bit 6 (P6) is 0, and the key code is usually 25H or 00101001B (it may also be other values, but it is definitely less than 40H) as shown in the following table, where the column scan code corresponding to DIG1 is 01B, and the row scan code corresponding to KI5 is 100B. The microcontroller can read the key code at any time. If you need to know when the key is released, you can read the key code regularly through the query method until the key code bit 6 (P6) is 0.

Output value when the button is released: **(P6=0 when the button is released)**

KI	DIG4	DIG3	DIG2	DIG1
A/KI1	07H	06H	05H	04H
B/KI2	0FH	0E	0D	0CH
C/KI3	17H	16H	15H	14H
D/KI4	1FH	1EH	1DH	1CH
E/KI5	27H	26H	25H	24H
F/KI6	2F	2EH	2DH	2CH
G/KI7	37H	36H	35H	34H
KI1+KI2	3FH	3E	3DH	3CH

Note: 1 The essential difference between the key code read when a key is released and when a key is pressed is whether bit 6 (P6) is 1.

2 After the key is released, it is usually as shown in the above table. Other situations may occur, but it is definitely less than 40H.

5. Instruction Set Description

1.Data command settings

name	instruction MSB							LSB	explain	Command value
	B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**		
System Commands	0	1	0	0	1	0	0	0	Set system parameter command	48H
Read key commands	0	1	0	0	1	X	X	1	Read key data command	49H

Note: The instructions used in this specification are hexadecimal H, and both input and read data start from the high bit. The bits marked with × can be 1 or 0, and it is recommended to write 0. Others must be fixed values.

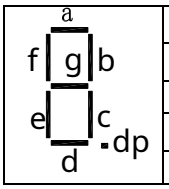
2.System parameter settings

name	instruction MSB							LSB	explain	Command value
	B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**		
Brightness settings	0	0	0	0			0		8Level brightness (default)	00H
	0	0	0	1			0		1Level brightness	10H
	0	0	1	0			0		2Level brightness	20H
	0	0	1	1			0		3Level brightness	30H
	0	1	0	0			0		4Level brightness	40H
	0	1	0	1			0		5Level brightness	50H
	0	1	1	0			0		6Level brightness	60H
	0	1	1	1			0		7Level brightness	70H
Segment Mode	0				0		0		8Segment output (default)	00H
	0				1		0		7Segment Output	08H
Working Mode	0					0	0		Normal working mode	00H
	0					1	0		Standby working mode	04H
Switch mode	0						0	0	Screen off display	00H
	0						0	1	Open screen display	01H

Note: Before sending the above system parameter setting command, you need to enter the system command 48H first, such as 48H+10H+01H=1 level brightness screen display **3. Video memory address**

name	instruction MSB LSB								Display address value
	B7	B6	B5	B4	B3	B2	B1	B0	
	DP/KP	G/KI7	F/KI6	E/KI5	D/KI4	C/KI3	B/KI2	A/KI1	
DIG1	0	1	1	0	1	0	0	0	68H
DIG2	0	1	1	0	1	0	1	0	6AH
DIG3	0	1	1	0	1	1	0	0	6CH
DIG4	0	1	1	0	1	1	1	0	6E

Note: According to the diagram7Common cathode drive circuit driver4Digital tube,DIG1-DIG4Display separately**1 2 3 4,**The data that the MCU needs to send is (68+06)+(6A+5B)+(6C+4F)+(6E+66); if you want to display**1.2.3.4.**You need to set the segment mode to 8-segment output first, and the data that the MCU needs to send is (68+86)+(6A+DB)+(6C+CF)+(6E+E6). When displaying decimals, it must be in 8-segment mode.



Display data															
0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**A**	**B**	**C**	**D**	**E**	**F**
3FH	06H	5BH	4F	66H	6DH	7D	07H	7F	6FH	77H	7CH	39H	5E	79H	71H
0.	**1.**	**2.**	**3.**	**4.**	**5.**	**6.**	**7.**	**8.**	**9.**	**A.**	**B.**	**C.**	**D.**	**E.**	**F.**
BFH	86H	DBH	CFH	E6H	EDH	FDH	87H	FFH	DFH	F7H	FCH	B9H	DEH	F9H	F1H

4. Segment mode and key indication

8-segment mode: DP/KP has the same function as KI1-KI7, both are used as segment outputs and can drive LEDs or digital tubes;

7-segment mode: KI1-KI7 can be used as segment output to drive LED or digital tube, and DP/KP pin is used as key scan mark output; in 7-segment mode and when the screen is on (48H+09H), when no key is pressed, DP/KP pin outputs high level, when a key is pressed, DP/KP pin will output low level, when the next key data is read (or the screen is turned off), DP/KP pin outputs high level.

5. Standby and wake-up

Standby: As long as the value of bit 2 (B2) in the system parameter setting command is 1, the chip will enter standby mode. In standby mode, the chip stops working, but the display data inside the chip will not change;

wake: After the chip enters standby mode, it can be awakened by the following methods: 1.

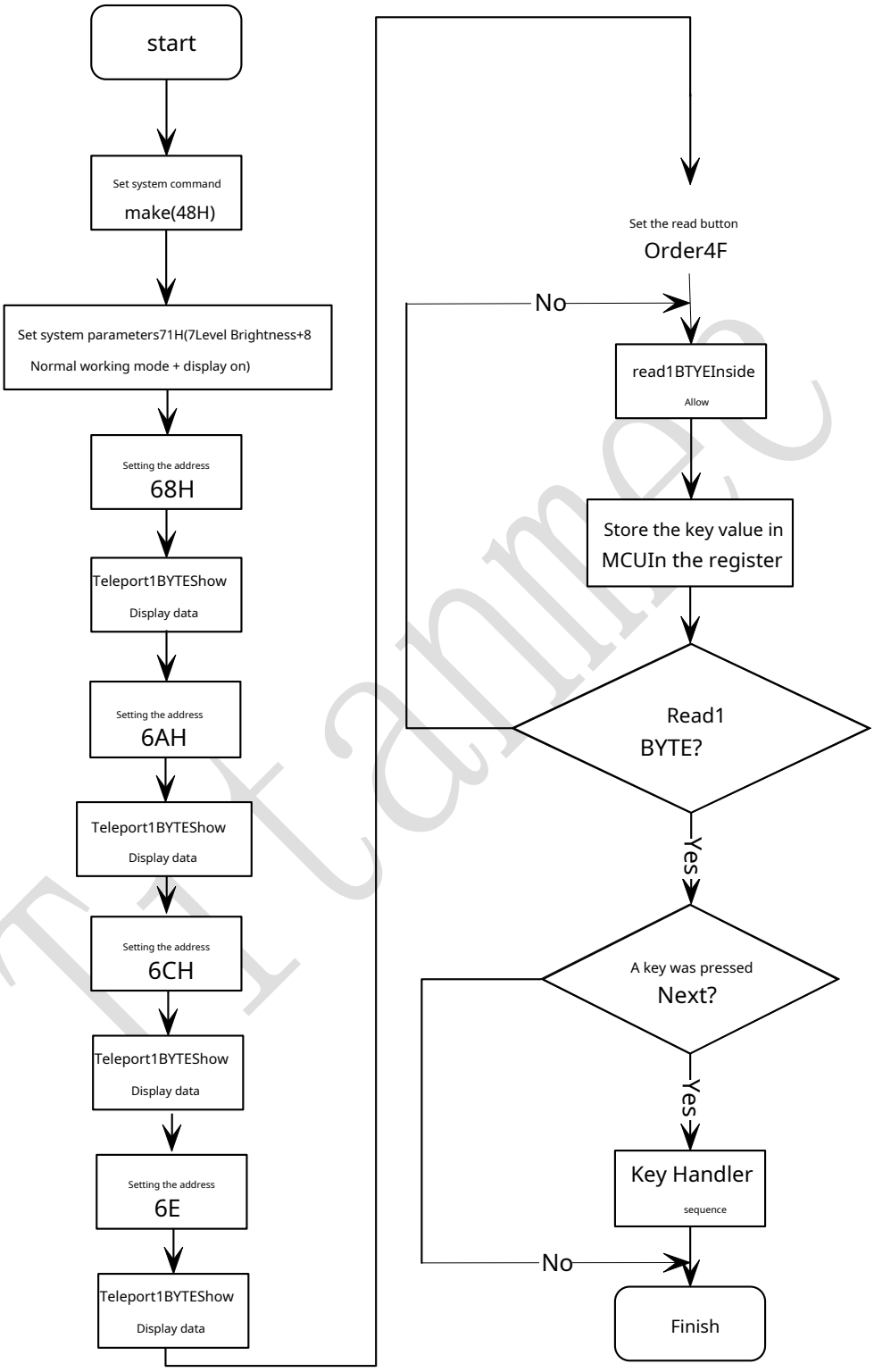
Send a non-standby mode system parameter setting command, such as 48H+01H (8 levels of brightness + normal mode + 8-segment mode + display on). The essence is to make the system parameter setting instruction bit 2 (B2) not 0;

2. The chip can be woken up by the key combination of KI1-KI4 and DIG1-DIG4. The key pressing time must be greater than 2 key scanning cycles. (80ms). Note: When the screen is off, you cannot observe whether the button can wake up the screen, so when using the button to wake up the screen, please use the standby command such as 48H+45H (4 levels of brightness + standby mode + display on).

6. Turning the screen on and off

Open screen: When the screen opening command is sent and it is in normal working mode, DIG1-DIG4 starts scanning; **Turn off the screen:**When the screen-off command is sent, the chip stops working, and the chip needs to be initialized again after the screen is turned on;

6. Complete operation flow chart:



Note: Customers can set system parameters according to actual needs.

7. Application circuit:

TM1650 drives the common cathode digital screen hardware circuit diagram 6:

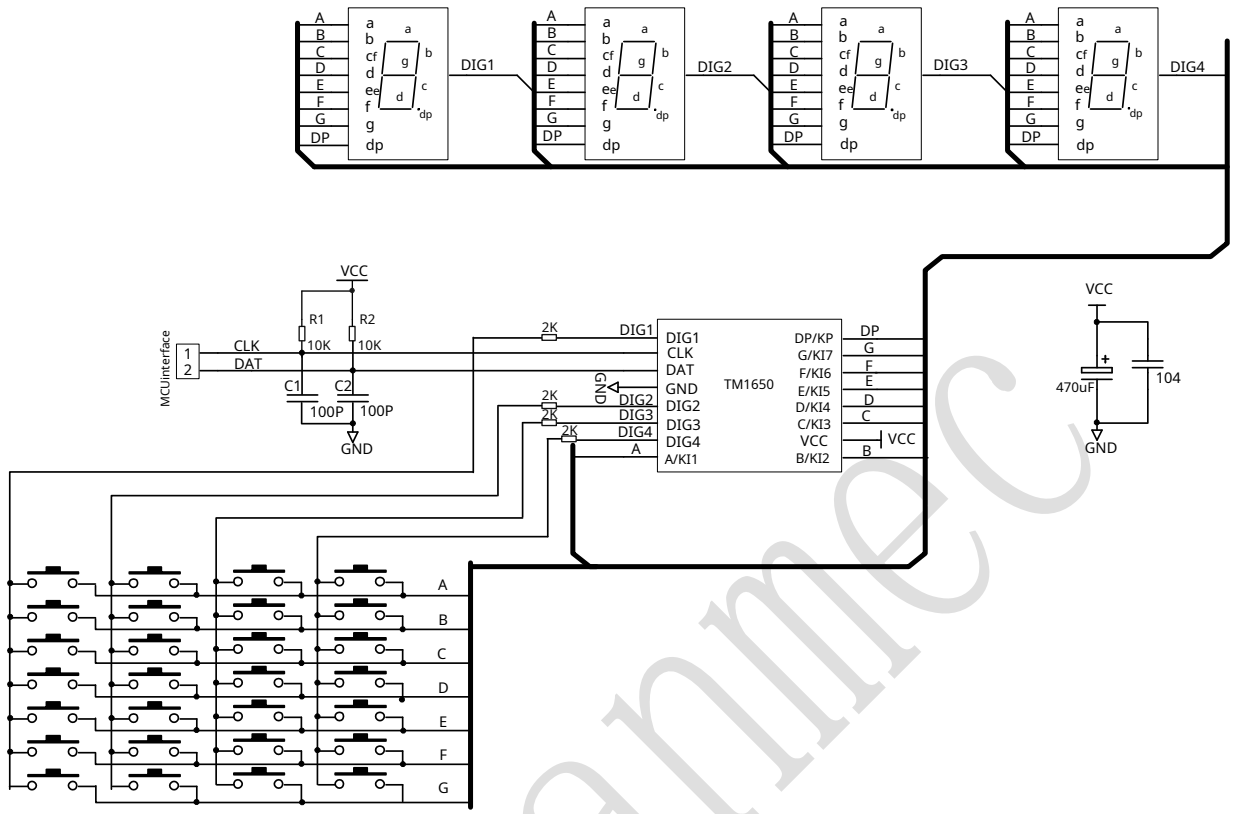


Figure 7 Common cathode drive circuit

▲ **Note**1. The filter capacitor between VDD and GND should be placed as close to the TM1650 chip as possible on the PCB board to enhance the filtering effect; minimize the loop area of the power supply and ground network, and provide a routing of no less than 0.5mm for the power supply and ground network.

2. DAT and CLK ports must be connected to pull-down capacitors, 100pF is recommended; pull-up resistors must be connected, 10KΩ is recommended. 3.

Since the on-state voltage drop of the blue-light digital tube is about 3V, the TM1650 power supply should be 5V.

4. When the chip works in a strong interference environment such as an induction cooker, it is recommended to appropriately reduce the communication frequency between TM1650 and MCU, and a 100Ω resistor can be connected in series on the communication port.

8. Electrical parameters:

Limit parameters (Ta = 25℃)

parameter	symbol	scope	unit
Logic supply voltage	VDD	-0.5～+6.5	V
Logic input voltage	VI1	- 0.5 ～ VDD + 0.5	V
LED segment driver output current	IO1	0 ～ 30	mA
LED driver output current	IO2	0 ～ 150	mA
Operating temperature	Topt	-40 ～ +85	℃
Storage temperature	Tsj	-65 ～+125	℃

Electrical(Test conditions: Ta = 25 ° C, V CC = 5V)

parameter	symbol	Minimum	typical	maximum	unit
Supply voltage	VCC	3	5	5.5	V
Supply Current	Ic	0.2	80	150	mA
Quiescent current (CLK, DAT, KP are high level)	Ics	-	0.3	0.6	mA
Standby current (CLK, DAT, KP are high level)	Ist	-	0.05	0.1	mA
CLK and DAT pin low level input voltage	VIL	- 0.5	-	0.8	V
CLK and DAT pin high level input voltage	VIH	2.2	-	VCC+0.5	V
KI pin low level input voltage	VIL(KI)	- 0.5	-	0.5	V
KI pin high level input voltage	VIH(KI)	1.8	-	VCC+0.5	V
DIG pin low level output voltage (-200mA)	VOL(DIG)	-	-	1.2	V
DIG pin low level output voltage (-100mA)	VOL(DIG)	-	-	0.8	V
DIG pin high level output voltage (5mA)	VOH(DIG)	4.5	-	-	V
KI pin low level output voltage (-20mA)	VOL(KI)	-	-	0.5	V
KI pin high level output voltage (20mA)	VOH(KI)	4.5	-	-	V
The remaining pins have low level output voltage (-4mA)	VOL	-	-	0.5	V
High level output voltage of other pins (4mA)	VOH	4.5	-	-	
KI pin input pull-down current	IDN1	- 30	- 50	- 90	uA
CLK pin input pull-up current	IUP1	10	200	300	uA
DAT pin input pull-up current	IUP2	150	300	400	uA
KP pin output pull-up current	IUP3	500	2000	5000	uA
Default voltage threshold for power-on reset	VR	2.3	2.6	2.9	V

Internal timing parameters (test conditions: Ta=25℃, VCC=5V)

parameter	symbol	Minimum	typical	maximum	unit
Reset time generated by power-on detection	TPR	10	25	60	ms
Display scanning cycle	TP	4	8	20	ms
Keyboard scan interval, key response time	TKS	20	40	80	ms

Note: The timing parameters in this table are multiples of the built-in clock period. The built-in clock frequency decreases as the power supply voltage decreases.

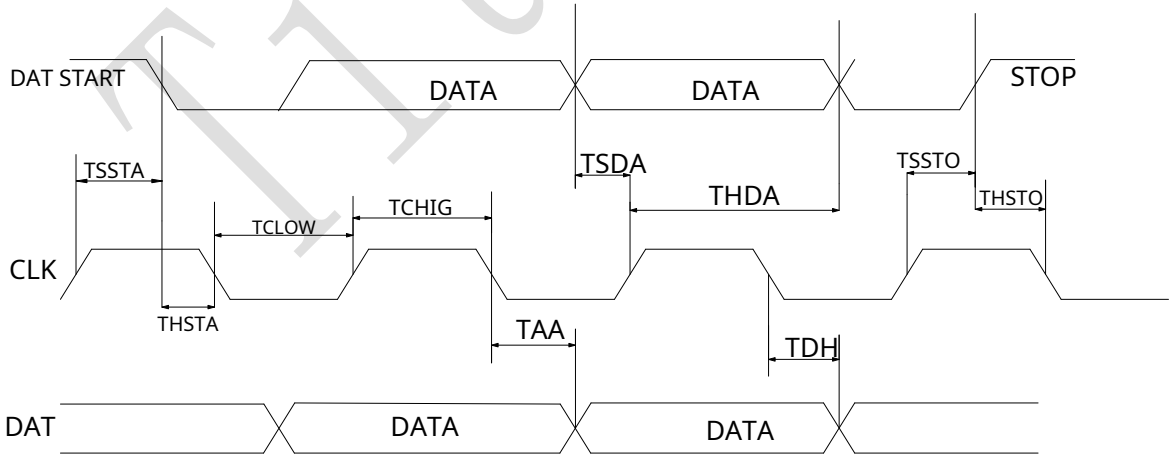
Timing characteristics (Ta = 25°C, VCC = 5V)

parameter	symbol	Minimum	typical	maximum	unit
DAT Falling edge start signal setup time	TSSTA	100	-	-	ns
DAT Falling edge start signal holding time	THSTA	100	-	-	ns
DAT rising edge stop signal setup time	TSST0	100	-	-	ns
DAT rising edge stop signal holding time	THST0	100	-	-	ns
CLK Low level width of the clock signal	TCLOW	100	-	-	ns
CLK High level width of the clock signal	TCHIG	100	-	-	ns
DAT Input data setup time for CLK rising edge	TSDA	30	-	-	ns
DAT Input data hold time for CLK rising edge	THDA	10	-	-	ns
DAT Output data valid delay to CLK falling edge	TAA	2	-	30	ns
DAT Output data invalid delay to CLK falling edge	TDH	2	-	40	ns
Average data transfer rate	Rate	0	-	4M	bps

Note: 1 The measurement unit of this table is nanosecond, i.e. 10$_{-9}$, if the maximum value is not specified, the theoretical value can be infinite.

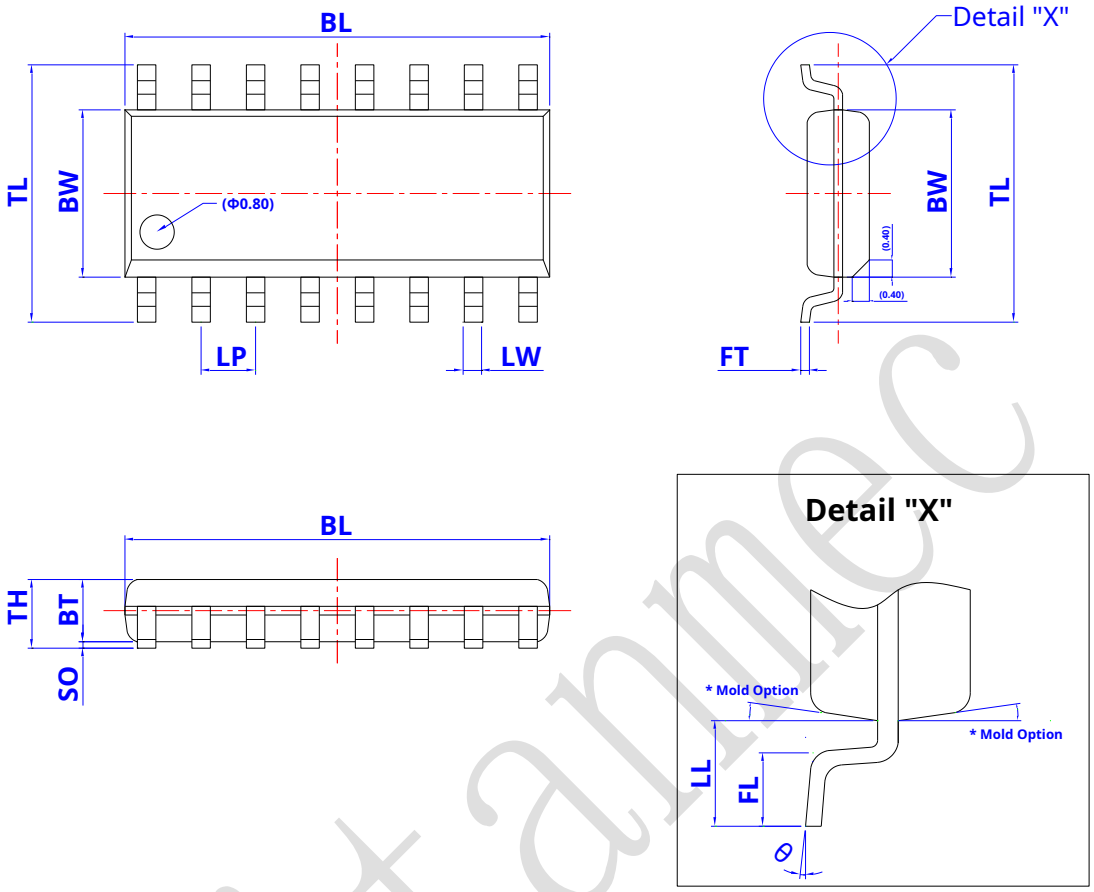
2 For different host computer platforms and hardware interface configurations, the average data transmission rate will vary greatly, and the recommended value is below 100KHz.

Timing waveform:



9. IC packaging diagram:

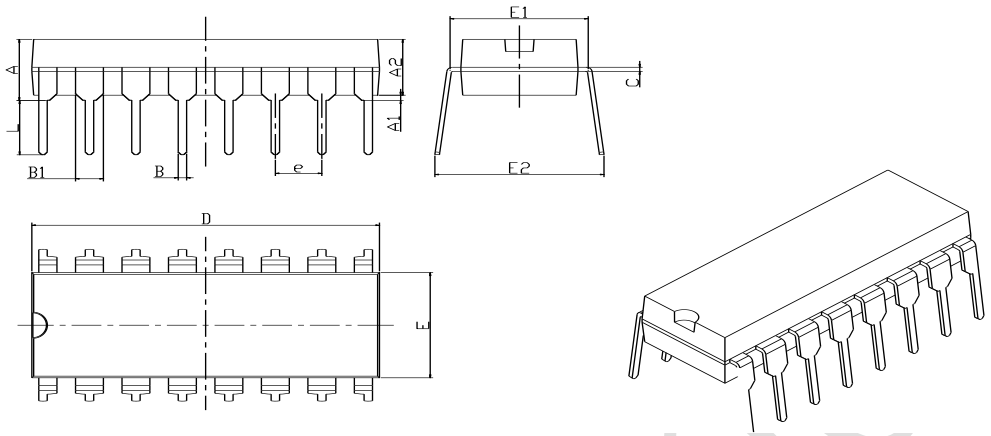
SOP16 Package Dimensions



Dimensions

Item	BL	BW	TL	LW	LP	FT	BT	SO	TH	LL	FL	Θ
express	Total length	Colloid width	span	Foot width	Foot spacing	Thick feet	Colloid thickness	Standing high	Colloid height	Single side length	Foot length	Foot Angle
Unit	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	?
Spec	10.00 (9.90) 9.80	4.00 (3.90) 3.80	6.20 (6.00) 5.80	0.430 TYP	1.270 TYP	0.250 (0.200) 0.150	1.55 (1.45) 1.25	0.200 (0.150) 0.060	1.650 Max.	1.25 (1.04) 0.80	0.80 (0.60) 0.45	8 (4) 0

DIP16 Package Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524(BSC)		0.060(BSC)	
C	0.204	0.360	0.008	0.014
D	18.800	19.200	0.740	0.756
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540(BSC)		0.100(BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

All specs and applications shown above subject to change without prior notice.

(The above circuits and specifications are for reference only. If our company makes revisions, we will not notify you separately.)